

The diagram illustrates a programmable logic device (PLD) architecture. It features a central crossbar array of programmable AND gates (10, 12, 14) and OR gates (16, 18, 20). The input lines V_A and V_B are connected to the AND gates. The output lines A and B are connected to the OR gates. The circuit is powered by V_{CCA} , V_{CCB} , and V_{CC} . Various components are labeled with numbers 1 through 42, including resistors, capacitors, and logic gates.

The diagram shows a differential pair of transistors, labeled 100, with gates tied together and biased at V_g . The threshold voltage is V_{th} . The source node is connected to a diode 104 and a resistor 106 in parallel. The diode 104 is connected to V_{cc} (labeled C), and the resistor 106 is connected to ground. The output of the diode branch is labeled S_0 . The differential outputs are V_A (labeled A) and V_B (labeled B).

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